REMARKS

Applicant respectfully requests reconsideration and allowance in view of the foregoing remarks. Claims 1-8, 10-14, and 33 are pending of which claims 1 and 33 are independent claims. In the Office Action mailed July 30, 2004, the Examiner rejected, among other things, claims 1, 5, 7, 8, 11, 12, 14 and 33 under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US 5,440,740) in view of Morton (US 5,822,606). The Examiner also rejected dependent claims 2-8 and 10-14 under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US 5,440,740), Morton (US 5,822,606), MacMillan et al. (US 6,278,707), Honary et al. (Publ. No. 2003/00464459 A1), Chauvel et al. (Publ. No. 2002/0078319 A1) and/or "Applicant's admitted prior art."

Claim Rejections under 35 U.S.C. §103(a)

Applicant's independent claim 1 recites a system for providing parallel processing of data to a plurality of digital signal processors (DSPs) that includes:

> means for transmitting communication data to a load management system from at least one CPU, wherein the load management system includes:
>
> > a plurality of direct memory access (DMA) devices, each DMA device having one or more internal registers, one or more FIFOs, and a state machine associated with the one or more FIFOs;
> >
> > a memory interface for interfacing the plurality of DMA devices with an external memory device;
> >
> > a plurality of status and control registers coupled to the plurality of DMA devices;
> >
> > at least one CPU interface for interfacing the at least one CPU with the plurality of status and control registers; and
> >
> > a plurality of DSP interfaces for interfacing the plurality of DSPs with the plurality of DMA devices;
>
> means for selecting two or more DSPs from the plurality of DSPs for processing the communication data;
>
> means for processing the communication data using the selected two or more DSPs; and
>
> means for transmitting the processed communication data back to the at least one CPU and to a communication device.

In the Office Action, the Examiner rejected claims 1, 5, 7, 8, 11, 12, 14 and 33 under 35 U.S.C. 103(a) as allegedly being unpatentable over Chen et al. (US 5,440,740) in view of Morton (US 5,822,606). Applicant respectfully traverses the rejection of these claims.

A §103(a), or obviousness, rejection is proper only when "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains." 35 U.S.C. §103(a). The Examiner must make out a *prima facie* case for obviousness. The mere fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness. The *en banc* Federal Circuit has held that "structural similarity between claimed and prior art subject matter, proved by combining references or otherwise, where the prior art gives reason or motivation to make the claimed compositions, creates a prima facie case of obviousness." *In re Dillon*, 16 U.S.P.Q. 2d 1897, 1901 (CAFC 1990). The underlying inquiries into the validity of an obviousness rejection are: "(1) the scope and content of the prior art; (2) the level of ordinary skill in the prior art; (3) the differences between the claimed invention and the prior art; and (4) objective evidence of nonobviousness." *In re Dembiczak*, 175 F.3d 994, 998, (Fed. Cir. 1999).

Further, the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990). Likewise, if the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984).

For at least the reasons stated below, Applicant asserts that the combination of the cited references fails to describe or suggest the subject matter as a whole of Applicant's claimed invention and, therefore, that Applicant's rejected claims are patentably distinct from the art of record.

Chen and Morton neither disclose nor suggest a system for providing parallel processing of data to a plurality of DSPs as recited, having a load management system that includes a

plurality of DMA devices, each having one or more registers, one or more FIFOs and a state machine associate with the one or more FIFOs, and a means for selecting two or more DSPs from a plurality of DSPs for processing communication data as required by independent claims 1 and 33.

First, Chen and Morton nowhere disclose a system having a "means for selecting two or more DSPs from a plurality of DSPs for processing the communication data." There are no teachings whatsoever in these references regarding "selecting two or more DSPs...for processing the communication data." The Examiner's cited passage of Chen at col. 31, lines 26-33 and figure 33 provides no discussion at all on this aspect of Applicant's invention. Each of Applicant's independent claims requires such selection of two or more DSPs. Further, Chen and Morton disclose a means for managing the use of the shared co-processor busses by only one co-processor sub-block at a time. With reference to Applicant's Figure 3B, Applicant's claimed invention does not incorporate this shared bus structure between the load management system 100 and the DSP array 12. Thus, parallel processing is facilitated.

Next, Chen and Morton nowhere disclose the parallel processing of communications data using two or more DSPs and the load management system as required by independent claims 1 and 33. Applicant's invention, for example as illustrated in Figure 3B, includes the means for utilizing two or more DSPs (via the load management system) working in parallel to process the communications data.

In summary, for at least the reasons presented above, Chen and Morton neither disclose nor suggest a system for providing parallel processing of data to a plurality of DSPs as recited, having a load management system that includes a plurality of DMA devices, each having one or more registers, one or more FIFOs and a state machine associate with the one or more FIFOs, and a means for selecting two or more DSPs from a plurality of DSPs for processing communication data as required by independent claims 1 and 33. Accordingly, Applicant respectfully submits that independent claims 1 and 33 are allowable over the art of record.

Dependent claims 2-8 and 10-14 ultimately depend from independent claim 1. The allowability of dependent claims 2-8 and 10-14 thus follows from the allowability of

independent claim 1; as such, dependent claims 2-8 and 10-14 are allowable over the art of record.

Conclusion

All rejections having been addressed, it is respectfully submitted that the present application is in a condition of allowance and a Notice to that effect is earnestly solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,
PILLSBURY WINTHROP LLP

Date: Nov. 30, 2004  42,727

Chang H. Kim Reg. No.
(650) 233-4776
REPLY TO CUSTOMER NO. 27498